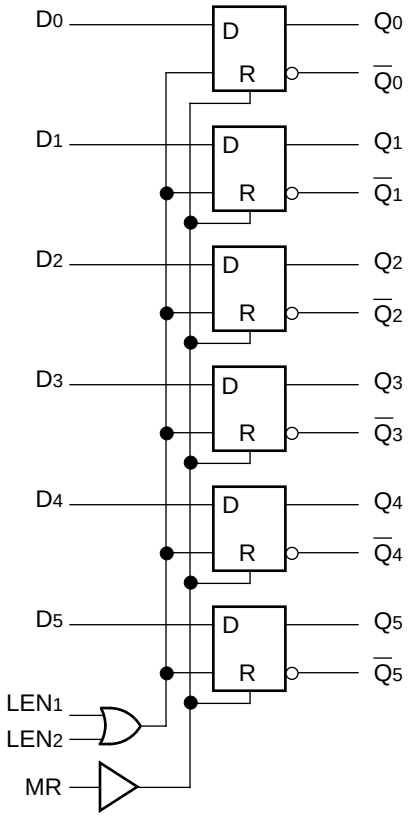
FEATURES

- **700ps max. propagation delay**
- **Extended 100E V_{EE} range of –4.2V to –5.5V**
- **Differential outputs**
- **Fully compatible with industry standard 10KH, 100K ECL levels**
- **Internal 75KΩ input pulldown resistors**
- **Fully compatible with Motorola MC10E/100E150**
- **Available in 28-pin PLCC package**

DESCRIPTION

The SY10/100E150 are 6-bit D latches with differential outputs designed for use in new, high- performance ECL systems. When both Latch Enables (LEN_1, LEN_2) are at a logic LOW, the latch is in the transparent mode and input data propagates through to the output. A logic HIGH on either LEN_1 or LEN_2 (or both) latches the input data. The Master Reset (MR) overrides all other signals to set the Q outputs to a logic LOW.

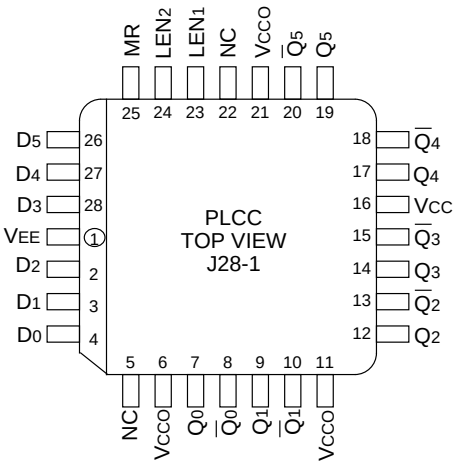
BLOCK DIAGRAM



PIN NAMES

Pin	Function
D_0–D_5	Data Inputs
LEN_1, LEN_2	Latch Enables
MR	Master Reset
Q_0–Q_5	True Outputs
$\overline{Q}_0$–$\overline{Q}_5$	Inverting Outputs
V_{CCO}	V_{CC} to Output

PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)

Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY10E150JC	J28-1	Commercial	SY10E150JC	Sn-Pb
SY10E150JCTR[2]	J28-1	Commercial	SY10E150JC	Sn-Pb
SY100E150JC	J28-1	Commercial	SY100E150JC	Sn-Pb
SY100E150JCTR[2]	J28-1	Commercial	SY100E150JC	Sn-Pb
SY10E150JZ[3]	J28-1	Commercial	SY10E150JZ with Pb-Free bar-line indicator	Matte-Sn
SY10E150JZTR[2, 3]	J28-1	Commercial	SY10E150JZ with Pb-Free bar-line indicator	Matte-Sn
SY100E150JZ[3]	J28-1	Commercial	SY100E150JZ with Pb-Free bar-line indicator	Matte-Sn
SY100E150JZTR[2, 3]	J28-1	Commercial	SY100E150JZ with Pb-Free bar-line indicator	Matte-Sn

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

TRUTH TABLE[1]

(Each Latch)

INPUTS				OUTPUTS		Operating
D_n	LEN_1	LEN_2	MR	Q_n	$\overline{Q}_n$	Mode
H	L	L	L	H	L	Latch
L	L	L	L	L	H	
X	X	H	L	Latched[2]	Latched[2]	
X	H	X	L	Latched[2]	Latched[2]	
X	X	X	H	L	H	Asynchronous

Notes:

1. H = HIGH state
   L = LOW state
   X = Don't care
2. Retains Data that is present before the LEN positive transition.

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

		T_A = 0°C			T_A = +25°C			T_A = +85°C				
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit	Condition
I_{IH}	Input HIGH Current										µA	—
	D	—	—	200	—	—	200	—	—	200		
	LEN MR	—	—	150	—	—	150	—	—	150		
I_{EE}	Power Supply Current										mA	—
	10E	—	52	62	—	52	62	—	52	62		
	100E	—	52	62	—	52	62	—	60	72		

AC ELECTRICAL CHARACTERISTICS

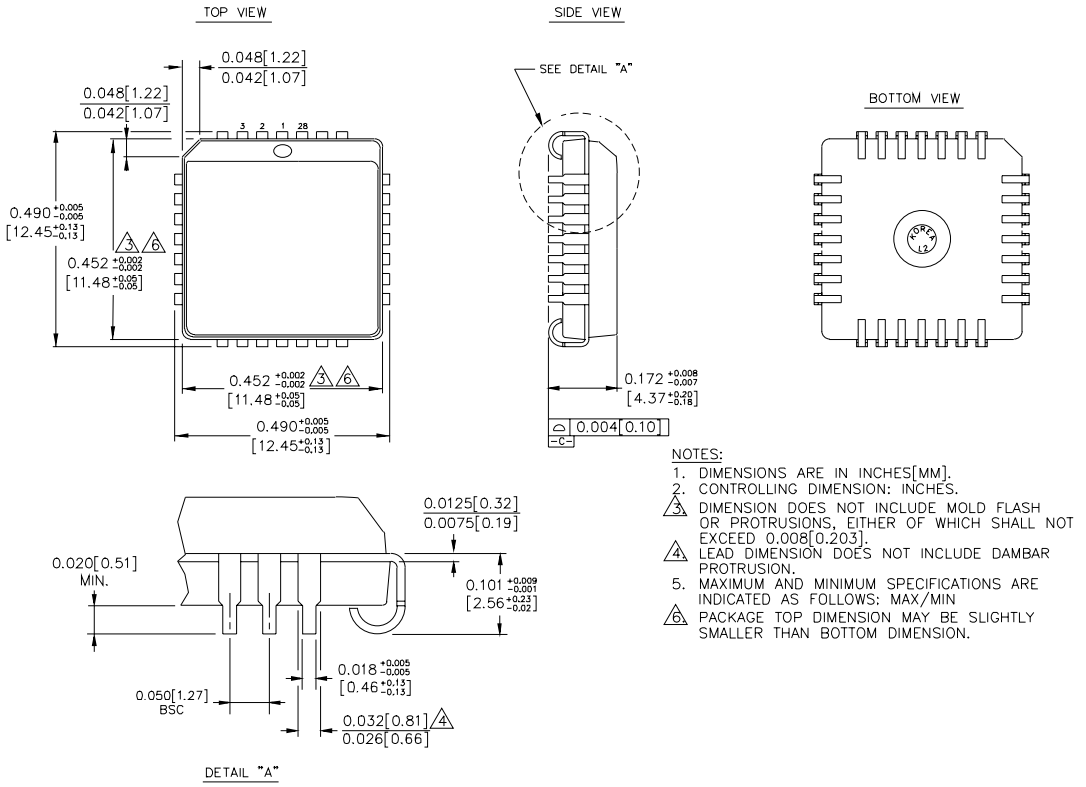
V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

		T_A = 0°C			T_A = +25°C			T_A = +85°C				
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit	Condition
t_{PD}	Propagation Delay to Output										ps	—
	D	250	375	550	250	375	550	250	375	550		
	LEN	375	500	700	375	500	700	375	500	700		
	MR	450	625	750	450	625	750	450	625	750		
t_S	Set-up Time, D	200	50	—	200	50	—	200	50	—	ps	—
t_H	Hold Time, D	200	–50	—	200	–50	—	200	–50	—	ps	—
t_{RR}	Reset Recovery Time	750	650	—	750	650	—	750	650	—	ps	—
t_{PW}	Minimum Pulse Width, MR	400	—	—	400	—	—	400	—	—	ps	—
t_{skew}	Within-Device Skew	—	50	—	—	50	—	—	50	—	ps	1
t_r t_f	Rise/Fall Time 20% to 80%	300	450	650	300	450	650	300	450	650	ps	—

Note:

1. Within-device skew is defined as identical transitions on similar paths through a device.

28-PIN PLCC (J28-1)



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