

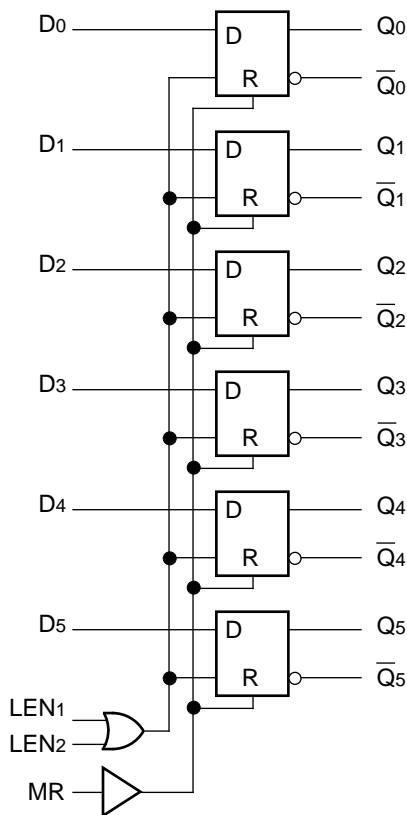
## FEATURES

- 700ps max. propagation delay
- Extended 100E VEE range of -4.2V to -5.5V
- Differential outputs
- Fully compatible with industry standard 10KH, 100K ECL levels
- Internal 75KΩ input pulldown resistors
- Fully compatible with Motorola MC10E/100E150
- Available in 28-pin PLCC package

## DESCRIPTION

The SY10/100E150 are 6-bit D latches with differential outputs designed for use in new, high-performance ECL systems. When both Latch Enables (LEN1, LEN2) are at a logic LOW, the latch is in the transparent mode and input data propagates through to the output. A logic HIGH on either LEN1 or LEN2 (or both) latches the input data. The Master Reset (MR) overrides all other signals to set the Q outputs to a logic LOW.

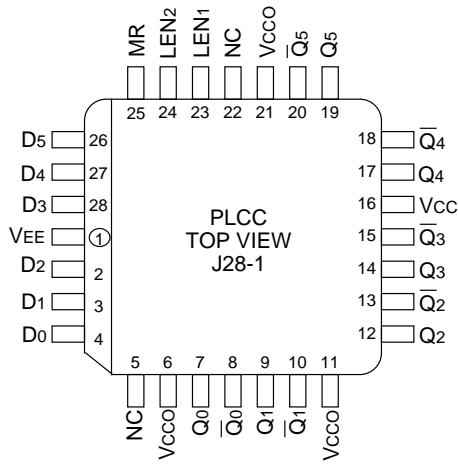
## BLOCK DIAGRAM



## PIN NAMES

Pin	Function
D0-D5	Data Inputs
LEN1, LEN2	Latch Enables
MR	Master Reset
Q0-Q5	True Outputs
$\overline{Q0}-\overline{Q5}$	Inverting Outputs
Vcco	Vcc to Output

**PACKAGE/ORDERING INFORMATION**



**28-Pin PLCC (J28-1)**

**Ordering Information<sup>(1)</sup>**

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY10E150JC	J28-1	Commercial	SY10E150JC	Sn-Pb
SY10E150JCTR <sup>(2)</sup>	J28-1	Commercial	SY10E150JC	Sn-Pb
SY100E150JC	J28-1	Commercial	SY100E150JC	Sn-Pb
SY100E150JCTR <sup>(2)</sup>	J28-1	Commercial	SY100E150JC	Sn-Pb
SY10E150JZ <sup>(3)</sup>	J28-1	Commercial	SY10E150JZ with Pb-Free bar-line indicator	Matte-Sn
SY10E150JZTR <sup>(2, 3)</sup>	J28-1	Commercial	SY10E150JZ with Pb-Free bar-line indicator	Matte-Sn
SY100E150JZ <sup>(3)</sup>	J28-1	Commercial	SY100E150JZ with Pb-Free bar-line indicator	Matte-Sn
SY100E150JZTR <sup>(2, 3)</sup>	J28-1	Commercial	SY100E150JZ with Pb-Free bar-line indicator	Matte-Sn

**Notes:**

1. Contact factory for die availability. Dice are guaranteed at T<sub>A</sub> = 25°C, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

**TRUTH TABLE<sup>(1)</sup>**

(Each Latch)

INPUTS			MR	OUTPUTS		Operating Mode
D <sub>n</sub>	LEN <sub>1</sub>	LEN <sub>2</sub>		Q <sub>n</sub>	$\bar{Q}_n$	
H	L	L	L	H	L	Latch
L	L	L	L	L	H	
X	X	H	L	Latched <sup>(2)</sup>	Latched <sup>(2)</sup>	
X	H	X	L	Latched <sup>(2)</sup>	Latched <sup>(2)</sup>	
X	X	X	H	L	H	Asynchronous

**Notes:**

- H = HIGH state  
L = LOW state  
X = Don't care
- Retains Data that is present before the LEN positive transition.

**DC ELECTRICAL CHARACTERISTICS**

V<sub>EE</sub> = V<sub>EE</sub> (Min.) to V<sub>EE</sub> (Max.); V<sub>CC</sub> = V<sub>CC0</sub> = GND

Symbol	Parameter	T <sub>A</sub> = 0°C			T <sub>A</sub> = +25°C			T <sub>A</sub> = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I <sub>IH</sub>	Input HIGH Current D LEN MR	—	—	200	—	—	200	—	—	200	μA	—
I <sub>EE</sub>	Power Supply Current 10E 100E	—	52	62	—	52	62	—	52	62	mA	—
		—	52	62	—	52	62	—	60	72		

**AC ELECTRICAL CHARACTERISTICS**

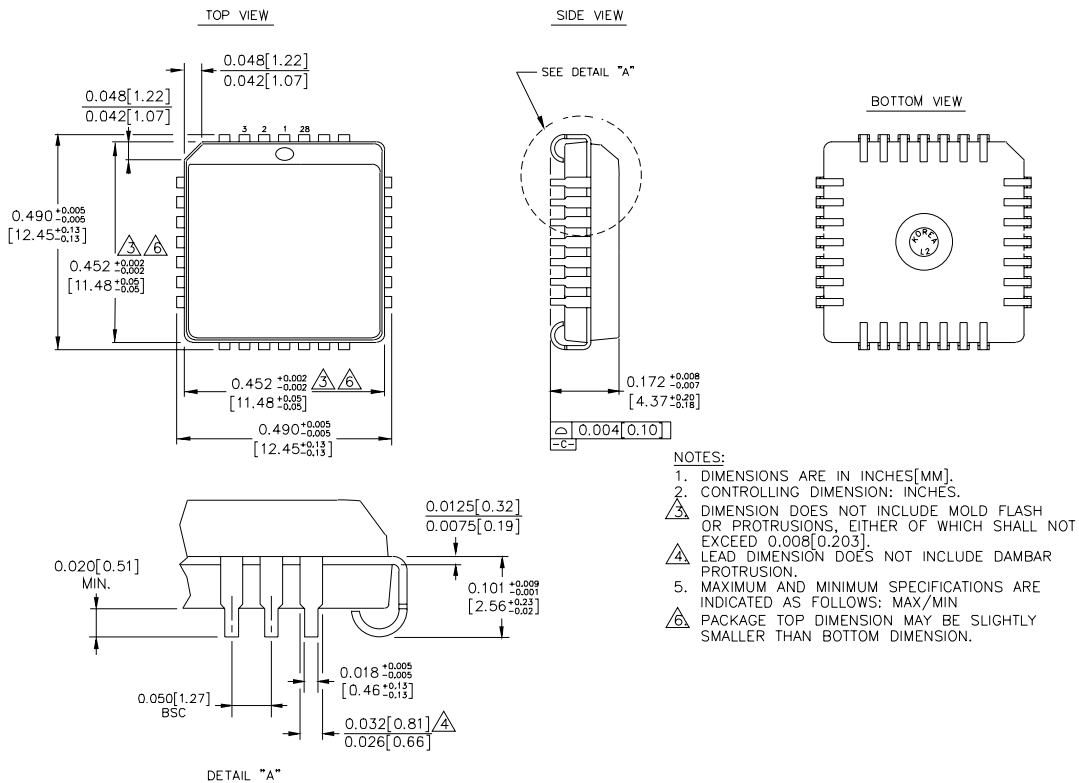
V<sub>EE</sub> = V<sub>EE</sub> (Min.) to V<sub>EE</sub> (Max.); V<sub>CC</sub> = V<sub>CC0</sub> = GND

Symbol	Parameter	T <sub>A</sub> = 0°C			T <sub>A</sub> = +25°C			T <sub>A</sub> = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t <sub>PD</sub>	Propagation Delay to Output D LEN MR	250	375	550	250	375	550	250	375	550	ps	—
t <sub>S</sub>	Set-up Time, D	200	50	—	200	50	—	200	50	—	ps	—
t <sub>H</sub>	Hold Time, D	200	-50	—	200	-50	—	200	-50	—	ps	—
t <sub>RR</sub>	Reset Recovery Time	750	650	—	750	650	—	750	650	—	ps	—
t <sub>PW</sub>	Minimum Pulse Width, MR	400	—	—	400	—	—	400	—	—	ps	—
t <sub>skew</sub>	Within-Device Skew	—	50	—	—	50	—	—	50	—	ps	1
t <sub>r</sub> t <sub>f</sub>	Rise/Fall Time 20% to 80%	300	450	650	300	450	650	300	450	650	ps	—

**Note:**

- Within-device skew is defined as identical transitions on similar paths through a device.

**28-PIN PLCC (J28-1)**



Rev. 03

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